

What is claimed is:

1 1. A communications interface, comprising:
2 a bus interface coupleable to a bus;
3 a plurality of transmit channels coupled to the bus interface;
4 a transmit control block coupled to the plurality of transmit channels;
5 a plurality of receive channels coupled to the bus interface; and
6 a receive control block coupled to the plurality of receive control
7 channels.

1 2. The communications interface of claim 1, further comprising a direct memory
2 access controller coupled to the bus interface.

1 3. The communications interface of claim 1, wherein the bus interface comprises a
2 plurality of transmit control registers and a plurality of receive control registers.

1 4. The communications interface of claim 3, wherein the plurality of transmit
2 control registers comprises at least one of:
3 an interface width register coupled to the transmit control block;
4 a transmit first in first out (FIFO) register associated with each transmit
5 channel;
6 an end of message (EOM) register associated with each transmit channel;
7 an interface interrupt identification register coupled to the transmit
8 control block;
9 a transmit frequency select register coupled to the transmit control block;
10 a wait count register coupled to the transmit control block;
11 a clock stop time register coupled to the transmit control block;
12 a channel configuration register associated with each transmit channel;
13 and
14 a channel status register associated with each transmit channel.

- 1 5. The communications interface of claim 3, wherein the plurality of receive
2 control registers comprises at least one of:
3 a receive FIFO register coupled to each receive channel;
4 an interface width register to select a predetermined number of bits to be
5 received across the communications interface by the receive control block;
6 a channel stop register associated with each receive channel;
7 a channel start register associated with each receive channel;
8 a wake up register associated with at least one receive channel;
9 an end of message register associated with each receive channel;
10 a channel configuration register associated with each receive channel;
11 and
12 a channel status register associated with each receive channel.
- 1 6. The communications interface of claim 1, wherein each of the plurality of
2 transmit channels and each of the plurality of receive channels comprises a first
3 in first out (FIFO) memory device.
- 1 7. The communications interface of claim 1, further comprising a power
2 management unit coupled to each of the plurality of transmit channels and
3 receive channels.
- 1 8. The communications interface of claim 1, wherein the transmit control block
2 comprises a channel arbiter adapted to select a next one of the plurality of
3 transmit channels to be activated.
- 1 9. The communications interface of claim 1, wherein the transmit control block
2 comprises a link controller adapted to transmit data from a selected transmit
3 channel across a selected link.

1 10. The communications interface of claim 1, wherein the receive control block
2 comprises a state machine adapted to store a current active channel number, a
3 number of bits in a current byte being transferred and to write each byte to a
4 selected one of the plurality of receive channels.

1 11. The communications interface of claim 1, wherein the plurality of transmit
2 channels comprises:
3 at least one channel adapted to send a clock signal;
4 at least one channel adapted to send a strobe signal;
5 at least one channel adapted to send a wait signal; and
6 at least one channel adapted to send data.

1 12. The communications interface of claim 1, wherein the plurality of receive
2 channels comprises:
3 at least one channel adapted to send a clock signal;
4 at least one channel adapted to send a strobe signal;
5 at least one channel adapted to send a wait signal; and
6 at least one channel adapted to send data.

1 13. The communications interface of claim 1, wherein at least one of the plurality of
2 transmit channels and the plurality of receive channels comprise a virtual general
3 purpose input/output channel.

1 14. The communications interface of claim 1, further comprising:
2 a channel stop threshold register adapted to set a threshold value to cause
3 a stop message to be sent to a source when a receive FIFO is full; and
4 a start threshold register adapted to set a start threshold value to cause a
5 start message to be sent to a source when the receive FIFO can receive additional data.

- 1 15. The communications interface claim 1, further comprising:
2 a stop message channel coupled to the receive control block and adapted
3 to send a stop message to a source when a receive FIFO reaches a stop threshold value;
4 and
5 a start message channel coupled to the receive control block and adapted
6 to send a start message to the source when the receive FIFO reaches a start threshold
7 value.
- 1 16. The communications interface of claim 1, further comprising at least one of a
2 direct flow control mode and a message flow control to control a flow of data
3 across the communications interface.
- 1 17. The communications interface of claim 1, wherein the transmit control block
2 comprises:
3 a multiplexer coupled to the plurality of transmit channels;
4 a parallel in serial out converter (PISO) coupled to the multiplexer; and
5 a control circuit coupled to the multiplexer and the PISO and adapted to
6 select one of the plurality of transmit channels to transmit data.
- 1 18. The communications interface of claim 1, wherein the receive control block
2 comprises:
3 a demultiplexer coupled to the plurality of receive channels;
4 a serial in parallel out converter (SIPO); and
5 a control circuit coupled to the demultiplexer and adapted to select one of
6 the plurality of receive channels to receive data.
- 1 19. An electronic system, comprising:
2 a first semiconductor chip;
3 a first communications interface coupled to the first semiconductor chip;

4 a second communications interface coupled to the first communications
5 interface, wherein each of the first and second communications interfaces include:
6 a bus interface coupled to the first semiconductor chip,
7 a plurality of transmit channels coupled to the bus interface,
8 a transmit control block coupled to the plurality of transmit
9 channels,
10 a plurality of receive channels coupled to the bus interface, and
11 a receive control block coupled to the plurality of receive control
12 channels; and
13 a second semiconductor chip coupled to the second communications
14 interface.

- 1 20. The electronic system of claim 19, further comprising at least one of a direct
2 flow control mode and a message flow control mode to control the flow of data
3 between the first chip and the second chip.
- 1 21. The electronic system of claim 19, wherein at least one of the first or second
2 semiconductor chips is a memory device and further comprising a direct
3 memory access controller coupled to between the memory device and the bus
4 interface.
- 1 22. The electronic system of claim 19, wherein the transmit control block comprises
2 a channel arbiter adapted to select a next one of the plurality of transmit
3 channels to be activated.
- 1 23. The electronic system of claim 19, wherein the transmit control block comprises
2 a link controller adapted to transmit data from a selected transmit channel to one
3 of the first or second semiconductor chips.

- 1 24. The electronic system of claim 19, wherein the receive control block comprises a
- 2 state machine adapted to store a currently active channel number, a number of
- 3 bits in a current byte being transferred and to write each byte to a selected one of
- 4 the plurality of receive channels.
- 1 25. The electronic system of claim 19, wherein each of the plurality of transmit
- 2 channels and each of the plurality of receive channels comprises:
 - 3 at least one channel adapted to send a clock signal;
 - 4 at least one channel adapted to send a strobe signal;
 - 5 at least one channel adapted to send a wait signal; and
 - 6 at least one channel adapted to send data.
- 1 26. The electronic system of claim 19, wherein at least one of the plurality of
- 2 transmit channels and one of the plurality of receive channels comprise a virtual
- 3 general purpose input/output channel.
- 1 27. The electronic system of claim 19, further comprising:
 - 2 a stop message channel coupled to the bus interface and adapted to send
 - 3 a stop message to one of the first or the second semiconductor chips when a receive
 - 4 FIFO reaches a stop threshold value; and
 - 5 a start message channel coupled to the bus interface and adapted to send
 - 6 a start message to the other of the first or the second semiconductor chips when the
 - 7 receive FIFO reaches a start threshold value.
- 1 28. A method of transmitting data between semiconductor chips, comprising:
 - 2 writing data into at least one of a plurality of transmit FIFOs;
 - 3 selecting one of the plurality of transmit FIFOs that contains data to be
 - 4 transmitted and that is not in a wait state; and
 - 5 transmitting the data to a corresponding one of the plurality of receive
 - 6 FIFOs that has not exceeded a threshold value.

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- 1 29. The method of claim 28, further comprising:
 - 2 sending a wait signal to a transmit control block if the corresponding one
 - 3 of the receive FIFOs cannot receive data; and
 - 4 removing the wait signal when the corresponding one of the receive
 - 5 FIFOs can receive data.
- 1 30. The method of claim 28, further comprising selecting another one of the
- 2 plurality of transmit FIFOs to send data to another corresponding one of the
- 3 plurality of receive FIFOs while the corresponding one of the receive FIFOs
- 4 cannot receive data.
- 1 31. The method of claim 28, further comprising:
 - 2 sending a strobe signal to initiate a transmission of data;
 - 3 sending a selected channel number over which the data is to be
 - 4 transmitted; and
 - 5 sending an end of message signal after the data has been transmitted.
- 1 32. The method of claim 28, further comprising:
 - 2 sending a stop message if the corresponding one of the receive FIFOs
 - 3 cannot receive data; and
 - 4 sending a start message when the corresponding one of the receive
 - 5 FIFOs can receive data.
- 1 33. The method of claim 28, further comprising:
 - 2 selecting one of the plurality of transmit FIFOs and the corresponding
 - 3 one of the plurality of receive FIFOs by a predetermined algorithm.
- 1 34. The method of claim 28, wherein the predetermined algorithm is round-robin.

1 35. The method of claim 28, further comprising selecting a interface width from one
2 of a serial width, a two-bit width and a nibble width.

1 36. A method of forming a communications interface, comprising:
2 forming a bus interface;
3 forming a plurality of transmit channels coupled to the bus interface;
4 forming a transmit control block coupled to the plurality of transmit
5 channels;
6 forming a plurality of receive channels coupled to the bus interface; and
7 forming a receive control block coupled to the plurality of receive
8 control channels.

1 37. The method of claim 36, wherein forming the bus interface comprises forming a
2 plurality of transmit control registers and a plurality of receive control registers.

1 38. The method of claim 36, wherein forming the transmit control block comprises:
2 forming a channel arbiter adapted to determine a next one of the plurality
3 of channels to be activated; and
4 forming a link controller adapted to transmit data from a selected
5 transmit channel across a selected link.

1 39. The method of claim 36, wherein forming the receive control block comprises
2 forming a state machine adapted to store a currently active channel number, a
3 number of bits in a current byte being transferred and to write each byte to a
4 selected one of the plurality of receive channels.

1 40. The method of claim 36, wherein forming the plurality of transmit channels and
2 forming the plurality of receive channels, each comprises:
3 forming at least one channel adapted to send a clock signal;
4 forming at least one channel adapted to send a strobe signal;

1 forming at least one channel adapted to send a wait signal; and
2 forming at least one channel adapted to send data.

1 41. The method of claim 36, further comprising forming at least one virtual general
2 purpose input/output channel.

1 42. The method of claim 36, wherein forming the transmit control block comprises:
2 forming a multiplexer coupled to the plurality of transmit channels;
3 forming a parallel in serial out converter (PISO) coupled to the
4 multiplexer; and
5 forming a control circuit coupled to the multiplexer and to the PISO.

1 43. The method of claim 36, wherein forming the receipt control block comprises:
2 forming a demultiplexer coupled to the plurality of receive channels;
3 forming a serial in parallel out converter (SIPO);
4 forming a control circuit coupled to the demultiplexer and adapted to
5 select one of the plurality of receive channels to receive data.